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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,703	07/12/2001	Kimihiko Fukawa	35.G2863	1531

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EXAMINER	
SAFAIPOUR, HOUSHANG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,703	FUKAWA, KIMIHIKO	
	Examiner	Art Unit	
	Houshang Safaipour	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 July 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 10-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Sakai et al. (U.S. Patent No. 4,875,099), and further in view of Tandon et al. (U.S. Patent No. 4,438,457).

Regarding claim 1, Sakai et al. discloses an image processing apparatus comprising: a plurality of sensor chips connected to one another formed on the same semiconductor chip (abstract, fig. 9). Sakai does not disclose a first pixel row having a plurality of pixels and a second pixel row having a plurality of pixels shifted with respect to the first pixel row. Tandon et al. discloses high-resolution imager employing such an arrangement (abstract, fig. 3). Therefore it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to combine these two inventions in order to increase the scan resolution due to the fact that the information between the photosites is detected by additional row of photosites.

Regarding claim 2, combination of Sakai and Tandon et al. disclose an image processing apparatus comprising: a plurality of sensor chips, each including a first pixel row and a second pixel row, which are formed on the same semiconductor chip, the first pixel row having a plurality of pixels arranged in a main scanning direction, and the second pixel row having a

plurality of pixels shifted along the main scanning direction with respect to the first pixel row (please refer to claim 1);

a combining circuit which selectively outputs a signal from the first pixel row and a signal from the second pixel row, wherein said combining circuit is common to said plurality of sensor chips; and a driving circuit which controls the sequential input of signals from said plurality of sensor chips to said combining circuit (Sakai, col. 3, line 31 through col. 4, line 25 and col. 2, lines 19-32).

Regarding 3, combination of Sakai and Tandon et al. disclose an image processing apparatus comprising: a plurality of sensor chips, each including a first pixel row and a second pixel row, which are formed on the same semiconductor chip, the first pixel row having a plurality of pixels arranged in a main scanning direction, and the second pixel row having a plurality of pixels shifted along the main scanning direction with respect to the first pixel row (please refer to claim 1);

Tandon et al. discloses a first output line provided outside said plurality of sensor chips, to which a signal from the first pixel row in each of the sensor chips is read; a second output line provided outside said plurality of sensor chips, to which a signal from the second pixel row in each of the sensor chips is read; a driving circuit, which drives said plurality of sensor chips to sequentially output signals to the first output line and the second output line; and a combining circuit provided outside said plurality of sensor chips, which selectively outputs the signals from the first output line and the second output line, wherein said combining circuit is common to said plurality of sensor chips (please refer to claims 1 and 2). Therefore it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to combine these two

inventions in order to increase the scan resolution due to the fact that the information between the photosites is detected by additional row of photosites.

Regarding claim 4, Sakai et al. discloses an image processing apparatus according to claim 2, further comprising an analog-to-digital converting circuit arranged to receive an output from said combining circuit (fig. 9, A/D 18).

Regarding claims 5-7 and 12-15 the arguments analogous to those presented for claim 4 are applicable to claims 5-7 and 12-15.

Regarding claims 10 and 11 the arguments analogous to those presented for claims 1-3 are applicable to claims 10 and 11.

Regarding claims 16 and 17 the arguments analogous to those presented for claim 8 are applicable to claims 16-17.

Regarding claims 18-22 the arguments analogous to those presented for claim 1 are applicable to claims 18-22.

Regarding claim 23, Sakai et al. discloses an image processing apparatus according to claim 1, further comprising: a light source, which emits light to an original document; and a lens array, which guides light reflected from the original document to said plurality of sensor chips (col. 2, lines 19-32).

Regarding claims 24-27 the arguments analogous to those presented for claim 23 are applicable to claims 24-27.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Sakai et al. (U.S. Patent No. 4,875,099), and in view of Tandon et al. (U.S. Patent No. 4,438,457) and further in view of Ang (U.S. Patent No. 6,507,011).

Regarding claim 8, neither Sakai nor Tandon disclose an image processing apparatus according to claim 2, further comprising: a first reference level adjusting circuit, which adjusts the reference level of the signal from the first pixel row; and a second reference level adjusting circuit, which adjusts the reference level of the signal from the second pixel row, wherein said first reference level adjusting circuit and said second reference level adjusting circuit are provided before said combining circuit. Ang discloses such an arrangement (fig. 2, col. 2 lines 49-58). Therefore it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to combine these three inventions for reference level adjustments.

Regarding claim 9, arguments analogous to those presented for claim 8 are applicable to claim 9.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Houshang Safaipour whose telephone number is (703)306-4037. The examiner can normally be reached on Mon.-Thurs. from 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward L Coles, Sr. can be reached on (703)305-4712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Houshang Safaipour
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Art Unit 2622
February 22, 2005

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